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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,449	07/18/2003	Nobuo Matsui	240541US2DIV	1115

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/16/2007.

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Office Action Summary	Application No.	Applicant(s)	
	10/621,449	MATSUI ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/865,289.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/621,449 filed 07/18/2003 and amendment filed 12/26/2006.

2. Claims 1-20 are pending in the Application. Claims 12-20 have been added to the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Objections

4. Claims 12-15, 20 are objected to because of the following informalities:

claims 12-15 line 2 after "instructions" delete "are" insert --is--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Killian et al. (US Patent 7,020,854).

With respect to claims 1 and 6 Killian et al. teaches a processor (col. 1, ll.15-20), a system LSI (col. 32, ll.40-50); comprising: a processor core (as shown on the Fig. 2 core processor 60 (col. 10, ll.31-39)); and a memory operatively coupled to said

processor (as shown on the Fig. 6, wherein core processor 60 (Fig. 2)/CPLD 202 coupled to various memory (col. 32, ll.62-67; col. 33, ll.1-7)); wherein said processor is designed (col. 9, ll.45-50) using the method comprising: selecting a cache size from given candidates (using configuration options such as selecting instruction/data cache size (col. 11, ll.63-64; col. 19, ll.40-47); selecting an instruction memory size from given candidates (col. 11, ll.60-62; col. 12, ll.15-17; ll.61-64); selecting a data memory size from given candidates (col. 43, ll.17-24); selecting at least one of a plurality of option instructions that are provided respectively in correspondence with machine instructions to be implemented within said processor core and described in general-purpose language (within designer-defined instructions using TIE instructions, which being flexible describe portion of the ISA and might be called general-purpose language as shown in the examples in the tables (col. 14, ll.19-61), wherein TIE code is related to C language (col. 27, ll.13-19; col. 30, ll.55-58; col. 35, ll.43-46)).

With respect to claim 10 Killian et al. teaches a method of generating a design of a system LSI using a description language (abstract; col., 64-66), comprising: preparing a configuration specifying a file including variable item definition information concerning a multiprocessor configuration (using a configuration manager screen 86 to design configurable processor based on a base processor description (col. 45, ll.28-30) as shown on the Fig. 3 and having an ability to create a new file or edit an existing file (col. 11, ll.10-23), including configurable instruction set architecture (ISA), wherein variable are used to describe instructions (col. 16, lli.47-60; col. 7, ll.25-28)); creating a customized description language mode (within generating a customized synthesizable

hardware description of the configurable processor (col. 10, ll.7-9)); and logically composing said design based on said description language model, wherein said variable item definition information contains at least one item of option instruction information and information concerning a user defined module and a multiprocessor configuration (within generating a configurable process design based on the base processor description, a base instruction set (col. 45, ll.28-30) and a plurality of configurable features including additional instruction in the configuration specification, which is different from the base instructions (col. 45, ll.30-41), wherein variables are used in describing set of instructions (col. 16, ll.47-60).

With respect to claim 16 Killian et al. teaches a method for designing a processor core used in a processor with a memory operatively coupled to the processor core (as shown on the Fig. 2 core processor 60 (col. 10, ll.31-39); and as shown on the Fig. 6, wherein core processor 60 (Fig. 2)/CPLD 202 coupled to various memory (col. 32, ll.62-67; col. 33, ll.1-7)), the method comprising: selecting a cache size from given candidates (using configuration options such as selecting instruction/data cache size (col. 11, ll.63-64; col. 19, ll.40-47); selecting an instruction memory size from given candidates (col. 11, ll.60-62; col. 12, ll.15-17; ll.61-64); selecting a data memory size from given candidates (col. 43, ll.17-24); selecting at least one of a plurality of option instructions that are provided respectively in correspondence with machine instructions to be implemented within said processor core and described in general-purpose language (within designer-defined instructions using TIE instructions, which being flexible describe portion of the ISA and might be called general-purpose language as

shown in the examples in the tables (col. 14, ll.19-61), wherein TIE code is related to C language (col. 27, ll.13-19; col. 30, ll.55-58)).

With respect to claims 2-5, 7-9, 11-15, 17-20 Killian et al. teaches:

Claims 2, 7 and 17: wherein said option instructions include a dividing option instruction (DIV) and a maximum/minimum value option instruction (MINMAX) (within "options" section menu shown on the display window of the Fig. 4, wherein configuration options are divided into plurality of options, for example "Implementation goals" (col. 11, ll.24-40), wherein each option instruction has minimum and maximum values such as "Target speed" from 100 MHz to 250 MHz (Fig. 4; col. 11, l.48; col. 19, ll.14-23);

Claims 3 and 8: wherein said processor core is provided with an instruction cache and a data cache (col. 11, ll.63-65);

Claims 4, 9 and 18: wherein said cache size, said instruction memory size, said data memory size, and said option instructions are provided in RTL templates (col. 33, ll.9-11);

Claims 5, 19: wherein said method further comprises selecting optional hardware associated with said processor (col. 17, ll.59-63);

Claim 11: wherein the description language comprises a hardware description language (HDL) (col. 7, ll.34-49);

Claims 12, 14, 20: wherein the plurality of option instructions is described in at least one of RTL description, behavior level description, and C/C++ model description (col. 31, ll.12-17; ll.44-48);

Claims 13, 15: wherein the plurality of option instructions is described both in RTL description and in behavior level description or C/C++ model description (col. 31, ll.12-17; ll.44-48);

Remarks

7. In remarks Applicant argues in substance:

a) As non-limiting examples, that general-purpose language can be a RTL description and behavior level description or C/C++ model description ... Killian does nor disclose or suggest such features.

b) Killian does not disclose or suggest such a feature: user defined instructions are described in a general-purpose language

c) With respect to the limitation "preparing a configuration specifying a file including variable item definition information concerning a multiprocessor configuration" rejection cites Killian at column 45, lines 28-30

d) Killian does not disclose or suggest the variable item definition information including "at least one item of option instruction information and information concerning a user defined module and a multiprocessor configuration

8. Examiner respectfully disagrees for the following reasons:

As to a) Killian et al. discloses the ISS (instructions set simulator) derives its decode and execution behavior form the same ISA (instructions set architecture) files used to define the hardware (RTL) and system software (col. 31, ll.14-17; col. 33, ll.32-34), wherein the ISS cache models are constructed by generating C code for the models (col. 31, ll.44-45).

As to b) Killian et al. disclose designer-defined instructions using TIE instructions, which being flexible describe portion of the ISA and might be called general-purpose language as shown in the examples in the tables (col. 14, ll.19-61), wherein TIE code is related to C language (col. 27, ll.13-19; col. 30, ll.55-58; col. 35, ll.43-46).

As to c) it has to be noted that aforementioned limitation rejection does not cite only column 45, lines 28-30, but states: "a configuration manager screen 86 to design configurable processor based on a base processor description (col. 45, ll.28-30) as shown on the Fig. 3 and having an ability to create a new file or edit an existing file (col. 11, ll.10-23), including configurable instruction set architecture (ISA), wherein variable are used to describe instructions (col. 16, lli.47-60; col. 7, ll.25-28) (see rejection of the claim 10).

As to d) Killian et al. disclose configurable instruction set architecture (ISA), wherein variable are used to describe instructions (col. 16, lli.47-60; col. 7, ll.25-28), including an ability of reusing of TIE descriptions (col. 41, ll.37-38).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Rossoshek
Examiner
Art Unit 2825

03/13/2007

STACY A. WHITMORE
PRIMARY EXAMINER